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Random-Telegraph-Signal Noise and Device Variability in Ballistic Nanotube Transistors

Neng-Ping Wang,[†] S. Heinze,*[,†] and J. Tersoff[‡]

Institute of Applied Physics, University of Hamburg, Jungiusstrasse 11, 20355 Hamburg, Germany, and IBM Research Division, T. J. Watson Research Center, Yorktown Heights, New York 10598

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ABSTRACT

In field-effect transistors (FETs), charge trapping in the gate oxide is known to cause low-frequency noise and threshold shifts. Here we calculate the effect of single trapped charges in a carbon nanotube FET, using the nonequilibrium Greens function method in a tight-binding approximation. We find that a single charge can shift and even rescale the entire transfer characteristic of the device. This can explain both the large "random telegraph signal" noise and the large variations between nominally identical devices. We examine the dependence on both the thickness and dielectric constant of the gate dielectric, suggesting routes to reduce electrical noise.

The past few years have seen remarkable progress in carbon nanotube field-effect transistors (CNFETs). High performance and even ballistic transport have been demonstrated,[1,2] and there is increasing focus on integrating such transistors into operational device circuits.[3,4] Device integration requires stable and uniform behavior of the individual transistors. However, all materials exhibit some low-frequency electrical noise,[5,6] and such noise increases inversely with the system size, so it is an especially serious problem in nanotubes.[7−10] For nanotube devices, there are also typically significant differences between nominally identical transistors, which pose an additional obstacle to integration.

For both nanotubes and common metal oxide semiconductor field-effect transistors (MOSFETs), low frequency noise can take the form of random telegraph signals (RTS), i.e., discrete switching between two (or more) levels of current, due to capture and emission of charges at individual traps in the oxide.[5,6,10] For RTS in silicon MOSFETs, the current variation rarely approaches 5%. For nanotubes, in contrast, giant RTS values of 60% or more have recently been reported,[10] with large amplitudes persisting even in the "on" regime of the device where noise is generally smallest. Large effects from single charges in CNFETs have also been found theoretically.[11,12]

The time constant for switching depends on many factors,[10] and in general each trap has a different time constant. When there are many traps with different time constants, the superposition of RTS leads to noise with approximately a $1/f$ dependence on frequency f.[5,6] Such "$1/f$ noise" is ubiquitous, and is especially large in nanotubes, where it has become the subject of intense study.[7−9,13] Understanding the effect of individual charge traps is a key step in developing a microscopic understanding of $1/f$ noise in CNFETs.

Just as charge switching of a single defect can lead to large RTS noise, a single trapped charge can significantly change the static device characteristics.[11,12] Such sensitivity may be a major factor in the large variations between nominally identical devices. Therefore, a better understanding of single-charge effects is a crucial step in designing nanotube circuits with uniformity among the individual transistors, as well as low noise.

Here, we investigate the effects of single charge traps on ballistic CNFETs, using the nonequilibrium Greens function method in a tight-binding approximation.[11] We focus on CNFETs with ohmic contacts, which are considered most desirable for high-performance devices.[2] We find that, for typical gate-oxide thicknesses, a single charge trap anywhere in the gate oxide can significantly change the device characteristics. If the charge state of the trap fluctuates, this leads to large RTS noise.

We find that the effect of a charge in the oxide can be approximated[12,13] as a shift in gate voltage V_g. Thus as V_g is varied, the noise becomes dramatically larger in the subthreshold regime, as is seen experimentally.[8,13] While V_g shifts are known to arise for macroscopic trapped charge, it is remarkable that a single charge can have such an effect.

If the charge is very close to the nanotube channel, then in addition to a shift, there is also a stretching of the gate-

* Corresponding author. E-mail: heinze@physnet.uni-hamburg.de.
[†] University of Hamburg.
[‡] IBM Research Division.

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voltage scale, leading to a reduction in subthreshold slope. This suggests that scattering by trapped charges may be an important though previously unrecognized factor limiting the subthreshold slope of nanotube devices. Also, in this case, even in the "on" regime we find RTS amplitudes up to 80%. Similar amplitudes have been seen experimentally.[10] In the subthreshold regime, the current variation can approach 100% for realistic oxide thicknesses.

We find that the sensitivity to trapped charge can be substantially reduced by using thinner gate dielectrics and by using high-*k* dielectrics. Thus sensitivity to noise can be included among other factors in optimizing the design of nanotube devices.

These results apply for a positive charge in a p-type device, or negative charge for n-type. For the reverse charge, we find that the effect is much weaker, with no threshold shift.

We use a self-consistent nonequilibrium Greens function method as described in detail in ref 11. We consider a zigzag (13, 0) carbon nanotube with a radius of 0.52 nm and a band gap of 0.68 eV. We use a cylindrical "wrap-gate" device geometry as shown in the insets of parts a and c of Figure 1. The nanotube is surrounded by a dielectric ($\epsilon = 3.9$ as for SiO_2) and a cylindrical gate at a radius R_g. The trapped charge is treated as effectively a point charge and is placed midway between the source and drain electrode.

Nanotube devices are typically p-type. We therefore take the work function of the metal source and drain electrodes to be 1 eV larger than that of the nanotube (measured from midgap). This gives an ohmic p-type contact, as has been obtained in recent experiments.[2,14,15] For n-type devices, the roles of positive and negative charges (and the signs of voltages) are reversed.

We first focus on a gate radius $R_g = 16$ nm, and a small drain voltage $V_d = 50$ mV. The transfer characteristics of the FET are shown in Figure 1 for different radial positions of the charge. We see that even a single trapped charge can shift the threshold voltage, and this shift becomes quite large when the charge is near the nanotube. Even a small shift leads to quite large changes in current in the subthreshold regime, where current is increasing exponentially with gate voltage.

We characterize the RTS noise amplitude by the fractional current change due to the trapped charge

$$A_{RTS} = (I_0 - I_Q)/I_0 \qquad (1)$$

where I_Q and I_0 are the current with and without the charge. As shown in Figure 1b, this change is largest in the subthreshold turn-on regime and remains large far into the on-state of the transistor. The RTS is most dramatic for a charge at the nanotube−oxide interface, where the amplitude reaches values close to 100%. While trapped charge can occur throughout the oxide, the nanotube−oxide interface is especially susceptible due to the absence of any oxide passivation in this system.

As we increase the distance of the charge from the nanotube, the RTS amplitude decreases as expected. However, it remains surprisingly large even at 3 nm or more.

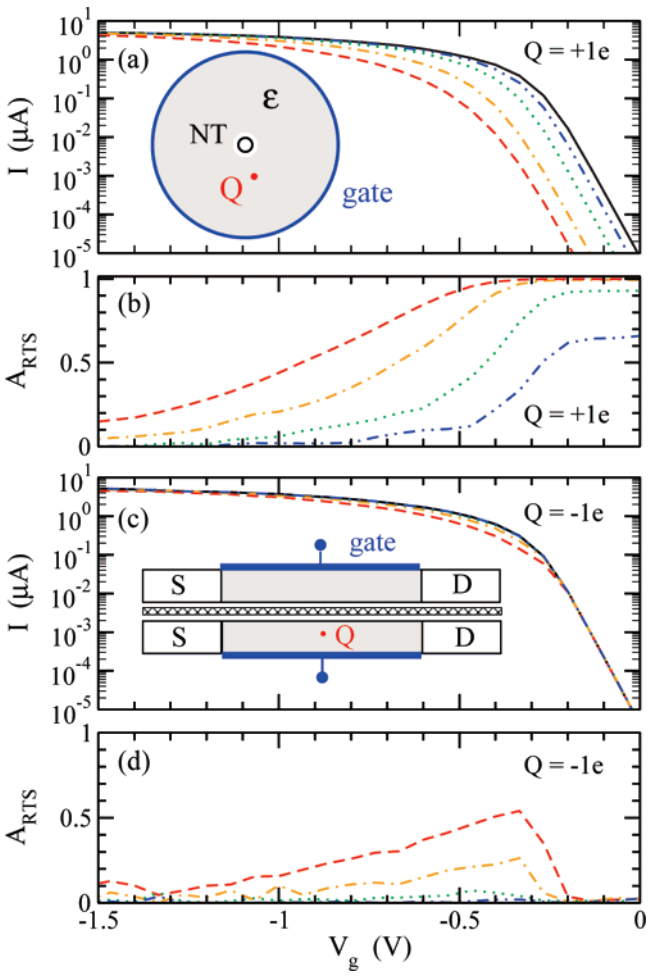

Figure 1. Effect of trapped charge on current, for different locations of the charge. Results are for a (13,0) carbon nanotube, with $V_d = 50$ mV, gate radius 16 nm, with SiO_2 as gate oxide. (a) Current vs gate voltage with no trapped charge (solid line), and for a positive charge at distances, from left to right, of 0.4, 1.4, 3.4, and 7.4 nm from the nanotube wall. (b) Relative current change for data of (a). (c, d) Same as (a, b), for negative charge. Insets of (a) and (c) show cross-sectional plots of the cylindrical geometry used in our calculation.

This is in good agreement with recent experiments[10] which reported giant RTS amplitudes of up to 60% in a broad regime of gate voltages for CNFETs in a planar geometry.

For a negative charge, parts c and d of Figure 1, the effect of the scatterer is much reduced. There is no threshold shift visible. While the Coulomb potential of a positive charge results in a barrier in the valence band and strong scattering of the holes, a negative charge creates a potential well and acts as a weaker scatterer. Within the turn-on regime, the RTS can still reach 50% for a trap at the nanotube−oxide interface. However, at larger distances the effect becomes small, and we do not further consider a negative charge in the following discussion. One should keep in mind, however, that the roles of positive and negative charges are reversed for an n-type nanotube transistor.

Figure 2 shows the dependence of RTS amplitude A_{RTS} on the radial position R_Q of a positive charge. For a charge near the nanotube ($R_Q \leq 3$ nm), A_{RTS} shows a simple exponential dependence on R_Q, which is perhaps not

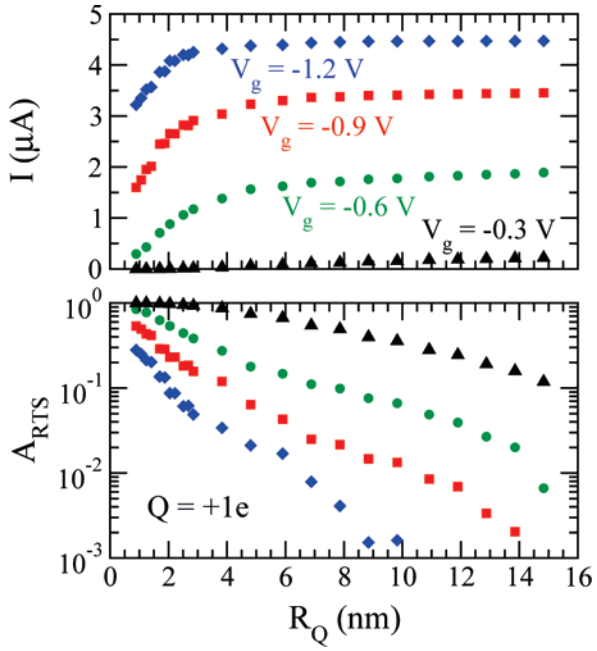

Figure 2. Current and noise vs radial charge position R_Q. Diamonds, squares, circles, and triangles correspond to gate voltages $V_g = -1.2$, -0.9, -0.6, and -0.3 V. $V_d = 50$ mV and $R_g = 16$ nm.

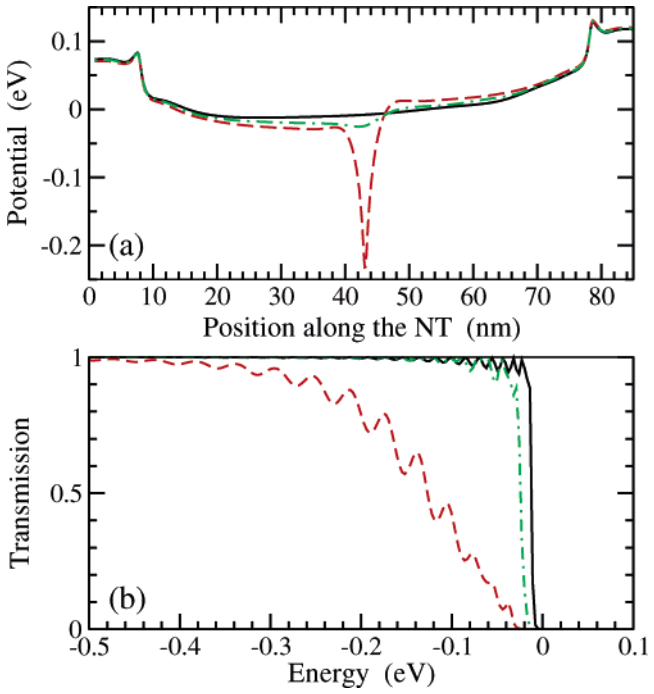

Figure 3. Potential and transmission at a gate voltage of $V_g = -0.5$ V and a drain voltage of $V_d = 50$ mV for the device considered in Figure 1. (a) Potential along the nanotube for $Q = 0$ (black solid curve), and for $Q = +1e$ at radial distances of 0.4 nm (red dashed curve) or 2.4 nm (green dashed-dotted curve) from the nanotube wall. (b) Transmission for the three cases defined in (a).

surprising since the current involves tunneling through the barrier created by the positive charge. The decay length $1/(\mathrm{d}\ln(A_{RTS})/\mathrm{d}R_Q)$ becomes shorter at full turn-on. At larger distances, the dependence on R_Q is modified, presumably due to screening of the charge by the gate.

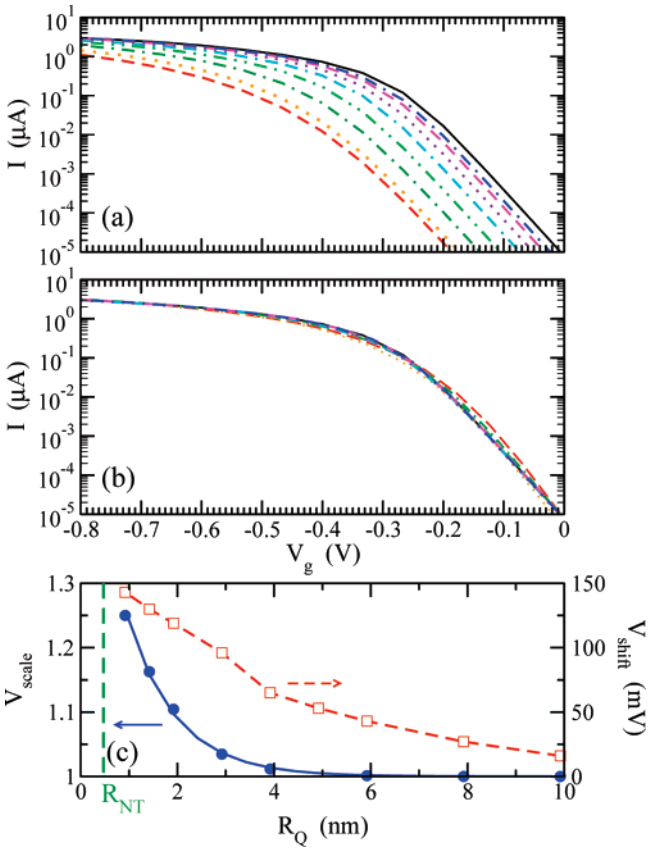

Figure 4. Scaling of the transfer characteristics with radial position of a positive charge in the oxide. The gate radius is 16 nm and the drain voltage is 50 mV. (a) Current for the charge at radial distances, from left to right, of 0.4, 0.9, 1.4, 2.4, 3.4, 5.4, 7.4, and 9.4 nm from the nanotube wall. The solid black line (top right curve) is the current in the absence of a scatterer. (b) Scaled and shifted curves of (a). (c) Scaling voltage (solid line) and voltage shift (dashed line) used to scale the curves in (b) vs radial charge position.

In order to understand the behavior, we examine the potential along the nanotube, Figure 3a. In the absence of a scatterer, the potential in the channel is almost constant in midchannel, as expected for a long-channel ballistic device. A positively charged trap located in the oxide 2.4 nm from the nanotube causes a broad shallow dip in the potential. Thus the valence-band edge that limits transmission of holes is determined by the *sum* of V_g and this extra dip, giving a shift in the plot of transmission vs energy, Figure 3b. This shifts the voltage threshold of the device, as seen in Figure 1a.

In contrast, a trapped charge right at the nanotube−oxide interface creates a large potential barrier that is much less flat. This gives a less abrupt turn-on of transmission with energy in Figure 3b. Therefore, we expect the effect to be more complex than a simple shift of V_g.

To explore this issue, we examine the effect of a trapped charge more quantitatively in Figure 4. Visually, the transfer characteristics in Figure 4a appear simply shifted, with charges near the nanotube giving larger shifts. However, we find that when the charge is very near the oxide surface, the curves in Figure 4a are stretched as well as shifted. Including both shifting and stretching gives a very good description, as confirmed in Figure 4b.

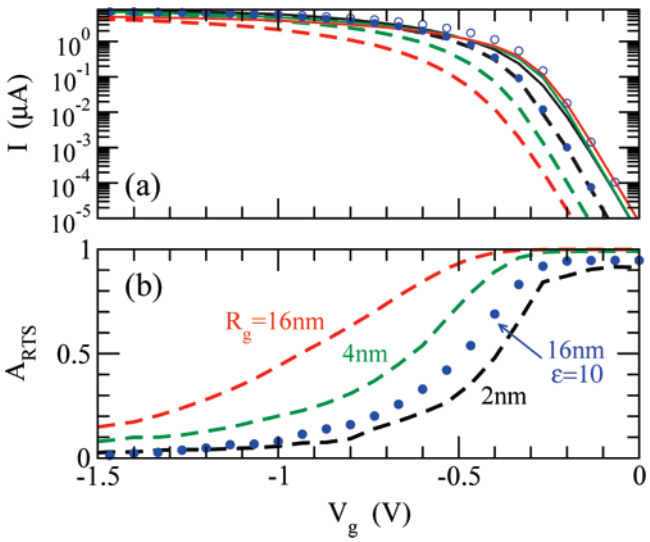

Figure 5. Effect of a trapped charge at the oxide surface, for different oxide thicknesses. (a) Current in the absence (solid curves) and in the presence (dashed curves) of a positive charge, for gate radii R_g of 2 nm (black curves), 4 nm (green curves), and 16 nm (red curves). (R_g = 2 nm corresponds to 1.2 nm oxide thickness.) (b) Relative current change for the cases shown in (a). In addition, (a) and (b) show the effect of using a gate dielectric ϵ =10, for the thickest oxide shown (blue open circles in (a) in the absence of a scatterer and filled circles in (a) and (b) in the presence of a scatterer).

We show the magnitude of the shift and stretch in Figure 4c. As expected, the voltage shift decreases smoothly with increasing distance of the charge from the nanotube. Moreover, a simple shift provides a good description for charges more than 3 nm from the nanotube. But for closer charges, the stretching is significant, reaching roughly 30% for charges right at the oxide surface. This corresponds to an increase of 30% in the subthreshold slope, a crucial measure of device performance which should be as small as possible. Thus trapped charge can degrade the performance in an additional and more subtle way than has been previously appreciated.

So far, we have concentrated on a single gate radius, i.e., a single gate-oxide thickness. In general, the performance of transistors is improved for reduced oxide thickness. We find that thinner oxides also reduce the effect of trapped charges. This is shown in Figure 5a. (The oxide thickness is $t_{ox} = R_g - 0.8$ nm.) Clearly, scattering from the charge is reduced with decreasing oxide thickness, resulting in smaller voltage shifts. Moreover, when the gate radius is reduced to 2 nm, the stretching of the gate voltage scale becomes negligible, $V_{scale} \approx 1$. (For radius 4 nm, V_{scale} is reduced to 1.1.) However, the threshold shift remains significant, giving large RTS amplitude (>50%) within the entire turn-on regime even for our ideal cylindrical geometry and the smallest gate radius considered. Presumably the improvement with smaller oxide thickness results in large part from improved screening of the charge by the gate electrode when the gate is closer.

Oxides with larger dielectric constant are another logical approach for reducing noise, since these also serve to screen the charge. As shown in Figure 5, even for a gate radius of 16 nm we can greatly reduce the RTS amplitude by using an oxide with larger dielectric constant, $\epsilon = 10$. The threshold voltage shift however still remains significant.

In conclusion, we have calculated large changes in ballistic carbon nanotube transistors due to single charges in the surrounding oxide. For p-type transistors, we observe dramatic current changes for individual positive charges and much smaller effects for negative charges, and vice versa for n-type contacts. We obtain giant amplitudes of RTS for charges in the vicinity of the nanotube, in agreement with recent experiments. Trapped charges lead to threshold shifts and gate voltage scaling of the transfer characteristics. Thinner gate oxides and high-*k* dielectrics can greatly reduce these effects.

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